REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-30 were pending. Claims 1-30 were rejected. Portions of the drawings were objected.

In this response, no claim has been canceled. Claims 1-4, 11-12, 17-18, and 24 have been amended. Portions of the specification have been amended. No new matter has been added.

Portions of the drawings are objected. In view of the foregoing amendments, it is respectfully submitted that the objections have been overcome.

Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. It is respectfully submitted that the claimed limitations are fully supported by the specification and drawings. For example, Figures 1A, 2, and 3, as well as their descriptions, clearly show that the host bus device and its virtual PCI device are not a host-to-PCI device. Nevertheless, in view of the foregoing amendments, it is respectfully submitted that the rejections have been overcome. Withdrawal of the rejections is respectfully requested.

Claims 1-3, 5-6, 9-12, 14-19, and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel 440BX AGPset: 82443BX Host Bridge Controller (hereinafter "Intel 82443BX") in view of U.S. Patent Number 6,629,157 by Falardeau et al. (hereinafter "Falardeau"). Claims 1-30 as amended include limitations that are not disclosed or suggested by the cited references, individually or in combination. Specifically, independent claim 1 recites as follows:

1. An apparatus, comprising:
an interface for directly coupling to a host bus having one or more processors without being shared with a host-to-PCI bridge;
a device coupled to the interface to perform one or more functions, said device appearing as a virtual PCI device logically residing on a PCI bus that is coupled to the host bus through the host-to-PCI bridge, wherein access by the device to the host-to-PCI bridge is only through the host bus; and
a monitor circuit coupled to said interface and said device to track host bus cycles initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device, and to generate one or more control signals to enable the device to respond, as the virtual PCI device, to said one or more of said identified host bus cycles targeted to said virtual PCI device without having to access the host-to-PCI bridge.

(Emphasis added)

Independent claim 1 includes an interface coupled to a host bus that is not shared with a host-to-PCI bridge and a device, where access of the device to the host-to-PCI bridge is only through the host bus. That is, the host bus device is located at the host bus separated from the host-to-PCI device. Further, the host bus device includes a monitor circuit that tracks the host bus cycles initiated by a processor on the host bus and routes the host bus cycles to the device without going through the host-to-PCI bridge. It is respectfully submitted that the above limitations are absent from the cited references, individually or in combination.

Rather, the Intel 82443BX discloses a host bridge having a host-to-PCI interface and a host-to-AGP interface (see, page iv of the Intel 82443BX), where the host-to-AGP interface is still considered as a host-to-PCI bridge (see, page 3-4 of the Intel 82443BX) and shares the host interface with the host-to-PCI interface. It appears that the Examiner interprets the host-to-PCI interface or the host-to-AGP interface of the Intel 82443BX as the host bus device as claimed in the present application. Specifically, the Examiner stated:

> "In regards to claim 1, 12, 18, 21, and 24-25: 82443BX teaches an apparatus comprising: an interface (Page iv Host Interface) for directly coupled to a host bus (Host bus) having one or more processors (Page iii multiprocessor support); a device (Page 3-5 "Virtual Host-to-PCI Bridge" identified as device 1 also the AGP interface

note 82443BX also has a device 0) coupled to the interface to perform one or more functions (AGP interface functions page 3-1), said device appearing as a virtual PCI device (82443BX calls it virtual) logically residing on a PCI bus (PCI bus 0) that is coupled to the host bus through a host-to-PCI bridge (Host-to-PCI bridge); and a monitor circuit (Decoder Page 1-2) coupled to said interface and said device to track host bus cycles (Host cycles) initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device, to said one or more said control signals (DEVSEL#) to respond, as the virtual PCI device, to said one or more said identified host bus cycles targeted to said virtual PCI device."

(Office Action, page 3, Emphasis added)

Applicant respectfully disagrees. Applicant respectfully submits that the present invention as claimed relates to a host bus device that physically sits on a host bus, but logically appears as a logical PCI device sitting on a PCI bus behind a host-to-PCI bridge (but not part of the bridge or a host-to-PCI bridge, such as, host-to-AGP bridge). In contrast, the Intel 82443BX is a bridge that provides interfaces to PCI buses and/or AGP devices, etc. The host-to-PCI and host-to-AGP interfaces are part of the host bridge coupling the host bus to other buses (e.g., a host-to-PCI bridge). Such interfaces are not the host bus devices as claimed in the present application that physically sit on the host bus and responds to the host bus cycles as a virtual PCI device without having to share with the host-to-PCI bridge. See, for example, Figure 1-1 on page 1-2 of the Intel 82443BX. Specifically, the Intel 82443BX states:

"The 82443 BX supports two bus interfaces: PCI (referred as Primary PCI) and AGP (referenced as AGP). The AGP interface is treated as a second PCI bus from the configuration point of view."

(Page 3-5 of the Intel 82443BX).

Thus, none of the interfaces can be considered as host bus devices as claimed in the present application. Applicant respectfully submits that, at most, the Intel 82443BX bridge as a whole, which couples a host bus to other buses, may be considered as a host bus device directly coupled to the host bus or a host-to-PCI or a host-to-AGP bridge, where the host-to-

AGP bridge is still considered as a host-to-PCI bridge (see, page 3-4 of the Intel 82443BX). However, the Intel 82443BX bridge cannot be considered as a virtual PCI device, other than a virtual host-to-PCI bridge, logically residing at a PCI bus behind a host-to-PCI bridge (within itself).

Even if, for the sake of the argument, that the host-to-PCI interface or the host-to-AGP interface may be considered as a host bus device directly coupled to a host bus, the Intel 82443BX still lacks a monitor circuit to track host bus cycles initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device (e.g., the alleged host bus device, such as the host-to-PCI interface or the host-to-AGP interface), and to generate one or more control signals to enable the device (again, the alleged host bus device, such as the host-to-PCI interface or the host-to-AGP interface) to respond, as the virtual PCI device, to one or more of the identified host bus cycles targeted to the virtual PCI device without accessing the host-to-PCI bridge.

The Examiner contends that a decoder of page 1-2 of the Intel 82443BX is the monitor circuit as claimed in the present application and the DEVSEL# signal is the control signal to enable a virtual PCI device to respond to the targeted host bus cycles. Applicant respectfully disagrees. The decoder of the Intel 82443BX does not track the host bus cycles that are targeted to the alleged host bus device when the device is considered either the host-to-PCI interface or the host-to-AGP interface. Rather, the alleged decoder decodes memory and IO cycles targeted to the memory or IO device (including the AGP device). Specifically, the Intel 82443BX states:

> "Host-initiated I/O cycles are decoded to PCI, AGP or PCI configuration space. Host-initiated memory cycles are decoded to PCI, AGP (prefetchable or non-prefetchable space) or DRAM (including AGP aperture memory). For memory cycles (host, PCI or AGP initiated) that target the AGP aperture space in DRAM, the 82443BX translates the address using the AGP address translation table. Other host cycles forwarded to AGP are defined by the AGP address map.
>
> (the Intel 82443BX, page 1-2, emphasis added).

Thus, importantly, Applicant respectfully submits that the host bus cycles are not targeted to the host-to-PCI interface or host-to-AGP interface. Rather, the host-to-PCI or host-to-AGP interface translates and forwards the host bus cycles from a host bus to PCI devices or AGP devices coupled to a PCI bus behind the host-to-PCI or the host-to-AGP bridge respectively, which is the target of the host bus cycles. However, the DEVSEL# signal is not a control signal that enables the host-to-PCI device or the host-to AGP device to respond, as the virtual PCI device, to one or more of the identified host bus cycles targeted to the virtual PCI device, because the host bus cycles are not targeted to the host-to-PCI or host-to-AGP bridge interface.

The AGP device asserts the DEVSEL# signal, not the host-to-PCI interface. Therefore, the monitor unit does not use the DEVSEL# signal to help the host-to-PCI interface to respond, but the other device coupled to the AGP interface.

Falardeau also fails to disclose the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over Intel 82443BX in view of Falardeau. Withdrawal of the rejections is respectfully requested.

Similarly, independent claims 12, 18, and 24 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claims 12, 18, and 24are patentable over the cited references.

Given that dependent claims 2-11, 13-17, 19-23, and 25-30 depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that claims 2-11, 13-17, 19-23, and 25-30 are patentable over the cited references.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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